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by

Luo Ying, Tang Shensheng

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PREPARED BY:

TRANSLATION SERVICES
NATIONAL AIR INTELLIGENCE CENTER
WPAFB, OHIO

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# DEVELOPMENT AND DESIGN OF DIGITAL RF MEMORY

Luo Ying Tang Shensheng

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ABSTRACT Digital radio frequency memory (DRFM) technology is capable of application in a good number of realms. In particular, in electronic countermeasure systems, it possesses the capability to carry out the acquisition and storage of received threat signals as well as capabilities associated with the precise control of wave forms for purposes of deception, and, in conjunction with that, obtaining the radiation to the threat object.

KEY WORDS +Digital radio frequency memory +Fast Sampling Electronic countermeasures Control Storage

## 1 INTRODUCTION

Electronic countermeasure systems require that jammers possess capabilities associated with the carrying out of acquisition and storage of received threat signal wave forms as well as capabilities for precisely controlling wave forms and, in conjunction with that, taking them and radiating them to the threat for purposes of deception. In early electronic countermeasure systems, option was made for the use of delay line methods to store pulse wave forms. However, this type of method is generally not able to maintain coherence between stored signals and received signals. Moreover, costs are expensive. Besides this, in areas associated with the realization of various types of deception technologies, it is also subject to very great limitations--for example, distance wave gate traction technologies associated with different pulse delay times. Following along with the appearance of coherent threat signals like pulse Doppler radar, it is necessary for electronic countermeasure systems to possess new processing methods capable of handling coherent wave forms.

Digital radio frequency memory (DRFM) technology, which appeared in the early 1980's, is capable of satisfying operational requirements for this type of multiple use method. It is able to store coherent signals of arbitrary length (linear modulation frequency pulse voltage, phase coding, and frequency coding). In conjunction with this, it produces distance wave gate traction or speed wave gate traction outputs. It is also possible to take signals representing base bands and transform them into digital bit flows stored in DRFM. Following that, they are "transferred". After going through a certain processing, signals are outputed. In this type of method, as far as DRFM is concerned--like digitally controlled frequency synthesizers--the frequency accuracies are

only related to sampling clocks and base oscillations. DRFM is also capable of being used in signal analysis--storage, analysis, and reproduction of wide band signals (frequency modulation, phase modulation, multiple simultaneous tone modulation, or other modulations).

At the present time, such countries as the U.S. and the U.K. are all actively engaged in DRFM research work. A good number of first generation DRFM products are just in the midst of production by such companies as Tasike (phonetic), Thunder ESD, as well as Design Engineering Laboratories, and so on. The majority of these products are still limited to single bit digitized forms. For example, in the ALQ-161 electronic warfare system, prepared for use on the U.S. B-1B model strategic bomber and which has already gone through successful development and into lot production, the first generation DRFM product associated with the most advanced radar capabilities, so as to improve jamming, has 500MHz sampling rates and 1 bit resolutions. However, single bit digitized forms limit the performance of DRFM. As a result, several teams--including among them the TRW company--are in the midst of developing high performance, multiple bit systems. In conjunction with this, they have gone into production in the early 1990's.

The future development of DRFM is to achieve higher sampling rates, higher resolutions, higher storage capacities, higher reliability, as well as low power consumption and cost. Moreover, GaAs technologies are very promising in this area. For this reason, a great many companies are all exerting efforts in research and development work associated with GaAs. For example, the TRW company will develop data selection/data distribution devices using 3GHz clock operations and 4 bit A/D memory devices as well as 4KRAM possessing 1ns access times. These will be typical components supplying the foundation for future second generation DRFM system technologies. /44

## 2 CIRCUITRY DESIGN AND TECHNOLOGICAL DIFFICULTIES

### 2.1 Circuitry Principles and Primary Functions

The basic functions associated with DRFM are to carry out samplings of inputed radio frequency signals. After that, on the basis of commands coming from control devices, they are then taken and converted into discrete analog values. Going through appropriate wave filtering, it is then possible to obtain initial base band signals. After that, through opting for the use of reference signals which are completely the same, the base band signals are converted into initial input coherent radio frequency signals. The line and block chart of the principles is as shown in Fig.1

On the basis of circuitry associated with these design principles, it should possess signal sampling, analysis, and recovery properties. It should possess the primary complete functions below.

a. Autoinspection of the complete system. Under the control of control devices, DMA operations are carried out. Read/write

memory and data confirmation channel operations are normal. In conjunction with this, initialization is carried out of the operations below.

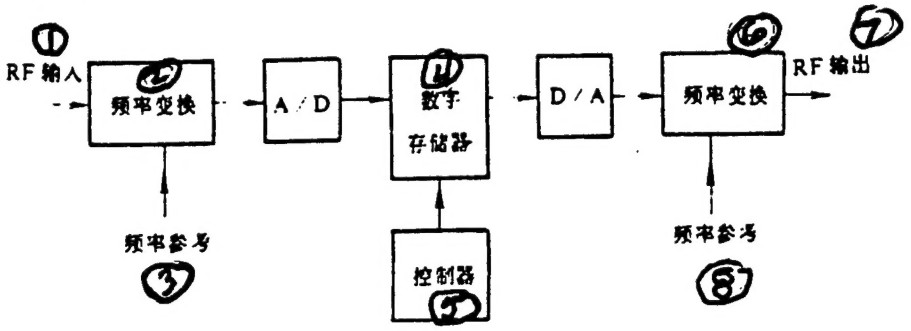


Fig.1 Diagram of DRFM Operating Principles

Key: (1) RF Input (2) Frequency Convertor (3) Frequency Reference (4) Digital Memory (5) Control Device (6) Frequency Convertor (7) RF Output (8) Frequency Reference

b. Under the control of control devices, high speed modulus conversions are carried out. In conjunction with this, data is transformed into memory match levels. After that, single channel data flows through data analyzers and is divided into two channels for storage into the two memory units A and B--causing comparatively low speed memory to match with high speed modulus transformation devices in terms of speed and electrical level.

c. After memory devices are stored full, computers are discontinued. DMA operations are carried out, reading in turn the contents of memory units A and B and forming a channel of data sent into computer internal storage in order to facilitate computers carrying out analysis and processing.

d. As far as the carrying out of DMA write operations is concerned, the data which is finished being processed and in internal computer storage is written in turn into memory units A and B in order to fully prepare for recovering signals.

e. Under the control of control devices, high speed modulus conversions are carried out, taking content in memory devices and recovering it into a channel of discrete analog values.

The various types of functions above are capable of being completed independently. They are also capable of arbitrary combination, carrying out operations in accordance with required sequences.

## 2.2 Design Difficulties and Solution Methods

### 2.2.1 Power Consumption

The selection of different devices determines the differing power consumptions possessed by systems. For example, speaking in terms of ECL memory devices, the power consumption per bit is on the order of 0.25mW. However, CMOS memory device power consumption is approximately 0.02mW per bit. There is a need to adopt memory devices with low power consumptions. However, low power consumption memory technology means read/write access times are comparatively slow.

### 2.2.2 Speed

The embodiment of the superiority of DRFM lies in the realizing of high speed sampling memory technology. The modulus convertor devices which are opted for in the circuit designs in question are the AD company's AD9002 product. Clock frequency is 100MHz. Resolution is 8 bits. Its data output is ECL levels. In order to realize low power consumption, option is made for the use of the concept of "pick fast and store slow". That is, making use of time division methods, one channel of high speed series link 8 bit data is divided into two channels stored in two memory units. In this way, memory device speed requirements are lowered by half.

### 2.2.3 Level Matching

Although time division methods solve speed problems, as a result, however, they also bring with them level matching problems. The reason is that high speed A/D outputs are ECL levels, but low power consumption memory devices are generally compatible with TTL levels. As a result, there is a need to introduce level switching circuits--that is, to take modulus transformer ECL outputs and change them into TTL levels, making them connect up with such other chips as memory devices. Moreover, this type of level switching circuitry possesses noise isolation functions. That is, it takes low noise ECL circuits and high noise CMOS or TTL circuits and separates them, causing modulus switching device operating environments to be good.

### 2.2.4 Time Sequencing

First of all, in circuits, use is made of several types of different clocks. During modulus number, number modulus switching, those used include ECL level and TTL level fast clocks as well as the internal computer clocks that are made use of when carrying out DMA operations. As a result, controllers should be able, on the basis of task commands, to select and supply correct clocks. Second, when data is changed from one channel into two channels or from two channels into one channel, it is necessary to guarantee correct time sequencing, making data and address changes match up with each other and guaranteeing data read/write stability and reliability. Besides this, data lines and address lines are common. When completing various functions, it should be guaranteed

that data lines are not subject to interference and memory device contents are not destroyed. In particular, in circuits of this type where operating speeds are comparatively high, the dangers of competition and risk taking are relatively great. Opting for the use of advanced programmable logic chips not only saves large amounts of logic gate circuitry and makes designs flexible. Moreover, it is capable of very, very greatly lowering the dangers associated with competition and risk taking.

### 2.2.5 Noise Suppression

Due to the fact that, in circuitry, clock frequencies are very high and logic relationships are complicated, and, moreover, they also include A/D and D/A circuits which are very sensitive to noise, as a result, requirements associated with antinoise properties in circuits are very high. Opting for the use of four layer board design, it is possible to very, very greatly improve circuitry properties. Besides this, when doing wiring, attention should be paid to the length of signal lead lines and symmetry relationships. In conjunction with this, option is made for the use of multiple point grounding methods. At the same time, selection should be made of appropriate common digital and analog points.

## 3 TESTS AND CONCLUSIONS

### 3.1 Tests

The circuitry design line and block chart is as seen in Fig.2.

In tests, signal sources are one linear frequency modulated source. The central frequency is 11.5MHz. Modulation band width is 1MHz. Contrasts are carried out of signal spectra measured by TF2370 spectrum analyzers and signal spectra calculated out in association with data sampling so as to check the properties of sampling data. In conjunction with this, empirical verification is made of the feasibility of using them in order to analyze such signal spectrum characteristics as linear frequency modulation, and so on.

Samplings of experimental data are used to do spectral analysis. In conjunction with this, frequency spectrograms are drawn out (omitted). From the graphs, it is possible to see that the central frequency of the signals in question is 11.4MHz. Band width is 1MHz. This is basically in line with TF2370 results.

### 3.2 Conclusions

In a good number of such realms as electronic warfare, DRFM technology possesses, in all cases, an important significance. This hardware circuitry design completes the core parts of DRFM. In conjunction with this, it possesses new characteristics.

Option is made for the use of the design concept "pick fast and store slow", and , in conjunction with that, ECL level high speed modulus switching devices and TTL level devices are made to link to each other. Problems associated with low device display speeds are resolved with the characteristics of power consumptions

that are small and low costs. Option is made for the use of advanced programmable logic control technology and simplified controller designs. In conjunction with this, competition and risk taking in circuitry are effectively prevented. Designs are perfected with regard to the links between microprocessors and circuit systems capable of carrying out flexible, sequenced control and completing multiple types of functions. /46

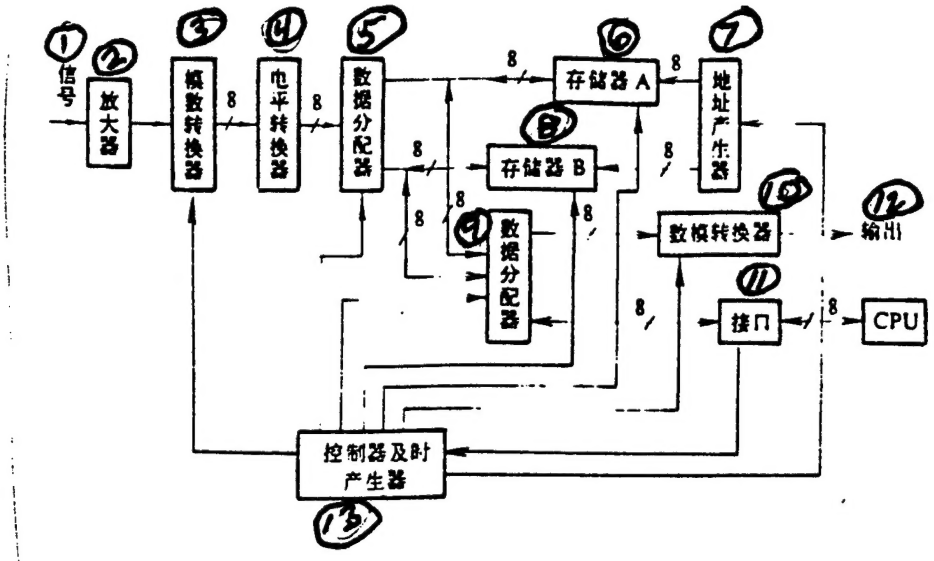


Fig.2 Circuitry Design Schematic

Key: (1) Signal (2) Amplifier (3) Modulus Number Converter (4) Level Converter (5) Data Distributor (6) Memory Device A (7) Address Generator (8) Memory Device B (9) Data Distributor (10) Number Modulus Convertor (11) Port (12) Output (13) Controllers and Time Generators

The systems in question are also capable of making a number of improvements. For example, opting for the use of orthogonal channels, it is possible to make signal analysis band widths increase one fold. Or, opting for the use of intermediate frequency direct sampling coherent wave detection technologies--that is, making use of single channel sampling signals--a number of processes are carried out on sample values, obtaining orthogonal I and Q values for the same instant and carrying out analysis.

Amounts of storage are increased in order to facilitate the carrying out of analysis on signals with comparatively long pulse widths.